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Review on Less Power Consumption by Noise Tolerant Circuit Technique for Dynamic Network

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Abstract: This paper presents a review on well known low power noise tolerant circuit technique for dynamic logic style. The main concern of this paper is to discuss the conventional domino logic style and to review the different approaches to overcome the drawback of conventional domino logic style. Different IC design techniques such as under the consideration of area, power and delay have been analyzed in this work.

Keywords: Domino logic, Dynamic Logic, Diode Footed Logic, Pull down Network.

INTRODUCTION

The exponential increment of current Integrated Circuit Design Techniques is due to its utilization in portable and wireless systems with in the form of low budgets and high performance microprocessor. To achieve this high performance the technology has been scaled down with its transistor size, area and supply voltage. But this approach increases the density of interconnection on reduced size chip. The use of clock in Dynamic Logic circuits also increases the density of the circuit in terms of interconnection. This High Clock frequency increases the capacitive coupling of the circuit. Therefore this leads to crosstalk and which is the main cause of

logic failure and delay of the circuit. There are other issues such as sub-threshold leakage current. Sub-threshold leakage current occurs when there is supply voltage is scaled then threshold voltage will also scaled which increased the leakage current. Due to continuous demand of high speed and small area devices the Dynamic logic are used in wide variety of applications because dynamic logic style is better than static logic style in terms of area and speed.

A dynamic Logic style contains a pull down network which realizes the desired logic function. The Dynamic logic works in two modes know as precharge and evaluation phase. The dynamic circuits precharged at every low edge of the clock and evaluates on every high edge of the clock. Therefore this clock is one of the sources of noise in dynamic logic circuit because of its high frequency, which also increases the power dissipation of the overall circuit.

CONVENTIONAL FOOTLESS DOMINO OR LOGIC

Conventional Domino logic style is better than static logic style in terms of speed and number of transistor in the circuit. The OR domino logic style is less noise tolerance which can cause the logic failure therefore one CMOS static inverter is used at the output stage of the inverter. As dynamic logic work in both precharge and evaluation phase .When the clock is low, the PMOS switched on and dynamic node is connected to the VDD or precharged to VDD. When clock is high in evaluation phase the dynamic node gets discharged though the pull down network if any of the input is high otherwise the dynamic node remains precharge. There are few draw backs associated with this logic such as Dynamic node leakage when all of the input transistors are logic low. This type of the leakage occurs in the case of when small noises at gate of NMOS pull down network or suthreshold leakage. This leakage is compensated by the use of PMOS keeper transistor which restores the voltage of dynamic node by adding the threshold voltage of it. The use of this extra PMOS keeper transistor increases the unwanted area of the chip because the area of PMOS usually 2 to 3 times of the NMOS transistors. Therefore the noise mainly depends on the gate to source voltage which some time increase because of the noise at the gate and dynamic nodes gets discharged.

PREVIOUSLY PROPOSED DOMINO OR LOGIC

The previously proposed domino OR logic is given in fig 2 [1] .In this circuit transistor M4 is used as stacking transistor. Therefore due to the stacking effect the gate to source voltage is reduced in the pull down network and this circuit have additional transistor M5 whose gate connected to clk.

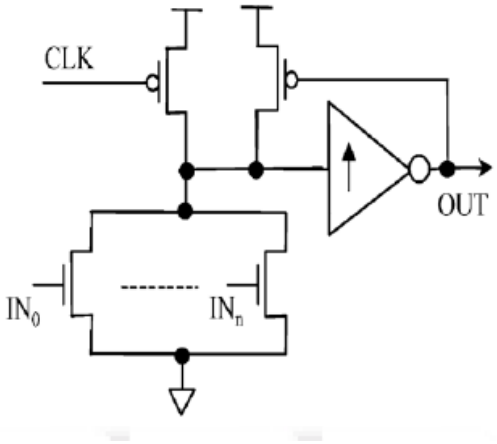

Fig 1: Conventional Footless Domino OR Logic

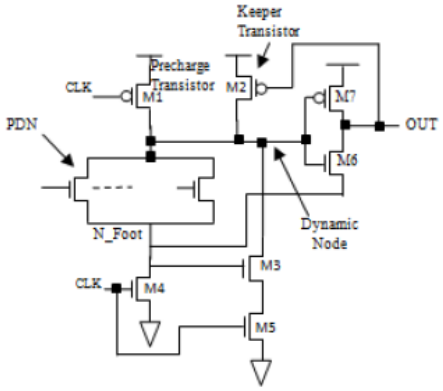

Fig 2: Previously Proposed Domino OR Logic

The use of extra M5 transistor is to reduce the leakage. When voltage drop occurs at 4 because of the noise at the input of Pull down Network. This causes the M3 is ON and M3 start leaking, therefore to reduce this leakage there has been used a M5 transistor in stack form to reduce the voltage drop which reduces the power dissipation of the circuit. The use of this circuit technique makes the circuit more noise robust and less power consuming but with some of the draw backs.

CONCLUSION

In this paper we have reviewed two different techniques for low power noise tolerant circuit designing. First techniques proposed a single keeper transistor to restore the dynamic node precharge voltage where as the previously proposed [2] domino OR logic style uses a different approach in which it uses three extra transistor in the pull down network. Therefore on the basis previous work one can propose a new noise tolerant circuit design techniques which can reduce discharging of dynamic node in precharge phase with the use of less number of transistors.

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